501.41197CX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): T. TAIRA

Serial No.: (not yet assigned)

Filed: September 26, 2003

For: FABRICATION METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND TESTING METHOD

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

September 26, 2003

Sir:

In the matter of the above-identified application, this information disclosure statement is being submitted with the following citation as specified in 37 CFR 1.97(d).

> "A copy of any patent, publication or other information listed in an information disclosure statement is not required to be provided if it was previously cited by or submitted to the Office in a prior application, provided that the prior application is properly identified in the statement and relied upon for an earlier filing date under 35 U.S.C. 120."

Applicant(s) are submitting herewith a copy of Form PTO-1449 which list documents cited in parent application(s) Serial No. 10/096,801, filed March 14, 2002.

Applicants offer the following comments:

(1) Sato, U.S. Patent No. 6,124,725, discloses a hybrid test method where a probe test (electrical characteristic test) and a burn-in test (reliability test) are performed in one prober to a single set of wafers, not to plural sets of wafers as recited in the claims of this application. Sato also neither discloses nor suggests any automatic test program which changes according to testing of different sets of

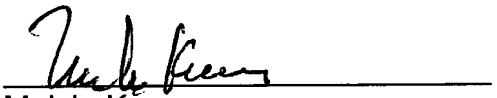
wafers. Furthermore, while Sato discloses an image data checking process of probing needles for wafer-probe alignment, Sato neither discloses nor suggests any image data checking processes of probing needle traces.

(2) Deckert et al, U.S. Patent No. 6,137,303, disclose an electrical test method where a plurality of wafer in one cassette are drawn out for the cassette (loading cassette) one by one, tested and accommodated in another cassette (unloading cassette). However, Deckert et al neither disclose nor suggest any electrical test method where the test object is automatically changed from one wafer set in one cassette to another wafer set in another cassette.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.41197CX1) and please credit any excess fees to such deposit account.

Respectfully submitted,



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Form PTO-1449 Equivalent	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 501.41197CX1 Serial No. (not yet assigned) Applicant: T. TAIRA Filing Date: September 26, 2003 Group:

U.S. Patent Documents

Examiner Initials	Document No.	Date	Name	Class Subclass	Filing Date If Approp.
	6,124,725	9/00	Sato		
	6,137,303	10/00	Deckert		

Foreign Patent Documents

	Document No.	Date	Country	Class Subclass	Translation Yes No
	5-136219	6/93	Japan		
	5-343497	12/93	Japan		

Other Documents (including Author, Title, Date, Pertinent Pages, etc.)

Examiner Date Considered

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.